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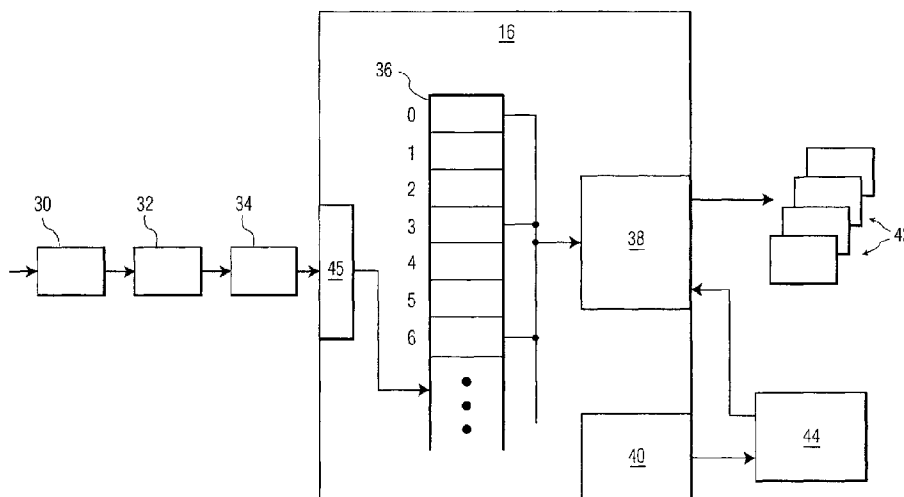
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(54) Title: COLOR BURST QUEUE FOR A SHARED MEMORY CONTROLLER IN A COLOR SEQUENTIAL DISPLAY SYSTEM



(57) Abstract: A system and method for managing the transfer of color data to a shared memory in a display processing circuit for use with a color sequential display. The system comprises a shared memory and a storage queue coupled to the shared memory, wherein the storage queue includes a system for receiving and storing alternating packets of color-specific video data in the storage queue. Also provided in the storage queue is a system for separately reading contiguous sets color-specific packets in bursts from the storage queue to the shared memory, e.g. DDR-SDRAM. To read color-specific packets to the shared memory, a system is employed in which a modulo-3 addressing system is used to select color specific sets of data. Alternatively a mapping system maps sequences of color packets to color specific portions of the memory.

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COLOR BURST QUEUE FOR A SHARED MEMORY CONTROLLER
IN A COLOR SEQUENTIAL DISPLAY SYSTEM

[0001] This application claims the benefit of copending provisional application 60/331,916 filed on November 20, 2001.

[0002] The present invention relates generally to memory storage in video display systems, and more particularly relates to a system and method for implementing a color burst queue for a shared memory controller in a color display system.

[0003] As the demand for devices having feature-rich video displays, such as laptops, cell phones, personal digital assistants, flat screen TV's, etc., continues to increase, the need for systems that can efficiently process video data has also increased. One of the many challenges involves managing the flow of video data from a video source to a video display. For example, systems: (1) may require different types of memory systems, including storage queues; (2) may utilize shared memory devices that require memory controllers to handle multiple real-time processes; (3) may be required to manage different types of data, etc.

[0004] A recent advance in video display technology in which the above-mentioned challenges arise involves color sequential display systems (i.e., color sequencing). Color sequencing utilizes a scrolling color architecture in which the red, green, and blue primary colors are sequentially presented to the same panel, using the same pixel locations. To implement such a system, the video data must be presented to the display panel at an elevated rate (e.g., a frame rate of 150-180 Hz) such that the viewer perceives a continuous full color image. The resulting speed and bandwidth requirements create challenges in designing an efficient low cost architecture for delivering video data from a source to the actual display.

[0005] For instance, storage queues that are used to buffer data going to or from a shared memory device are normally implemented as FIFO's (i.e., first-in first-out storage) or dual port memories that are addressed as FIFO's. In the case of a shared memory system that is used within a color sequential display, the color components must be separately processed, which implies three FIFO's, one for each color. This requirement of having three FIFO's adds to the cost and complexity of the

system. Accordingly, a system and method are required in which multiple FIFO's are not needed.

[0006] The present invention addresses one or more of the above-mentioned problems, by providing a storage queue for a color sequential display system comprised of a single dual port memory that stores and retrieves color-specific video data and provides color separation. In a first aspect, the invention provides a storage queue for a color sequential display system, wherein the storage queue is coupled to a shared memory and comprises: a system for receiving and storing individual packets of alternating red, green and blue video data in the storage queue; and a system that can read out separate sets of red packets, green packets and blue packets from the storage queue to the shared memory.

[0007] In a second aspect, the invention provides a method of managing color sequential display data in a storage queue that is coupled to a shared memory, comprising: receiving and storing individual packets of alternating red, green and blue video data in the storage queue; and reading out separate sets of red packets, green packets and blue packets from the storage queue to the shared memory.

[0008] In a third aspect, the invention provides a memory management system for use in a color sequential display, comprising: a shared memory; and a storage queue coupled to the shared memory, wherein the storage queue includes: a system for receiving and storing individual packets of alternating color-specific video data in the storage queue; and a system for bursting separate sets of color-specific packets from the storage queue to the shared memory.

[0009] These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

[0010] Figure 1 depicts an exemplary video processing circuit in accordance with the present invention.

[0011] Figure 2 depicts a memory control system for a storage queue in accordance with the present invention.

[0012] Figure 3 depicts an alternate embodiment of a memory control system for a storage queue in accordance with the present invention.

[0013] Figure 4 depicts a flow diagram of a read controller method in accordance with the present invention.

[0014] Referring now to the drawing, Figure 1 depicts a display processing circuit 10 for a color sequential display system that receives a source video 12 and outputs a display video 24. Along the processing chain, video data may be processed by a source processing system 14 and an intermediate processing system 20. In addition, a pair of storage queues 16 and 22 is utilized to temporarily store data. Finally, a shared memory 18 is included in the circuit as, for instance, a frame memory to increase the frame rate from the source rate to the display rate. (The ratio of the display to source rate is typically greater than 1.)

[0015] The shared memory 18 may be implemented using a double data rate synchronous dynamic random access memory (DDR-SDRAM). Source video 12 arrives at a regular rate and is stored in queue A 16 prior to being burst into the shared memory 18. Queue B 22 is read at a regular rate. A scheduler (described below) monitors the fullness 26, 28 of both queues and decides when bursts should occur in order to guarantee that neither queue underflows or overflows. The present invention describes a system for controlling the memory associated with a source storage queue (i.e., queue A 16). More particularly, the present invention describes a system and method that can efficiently burst sets of color specific video data from a storage queue to a shared memory. It should be understood that the display processing circuit of Figure 1 is depicted for exemplary purposes only, and other configurations utilizing the described invention in which a storage queue is coupled to a shared memory fall within the scope of the present invention.

[0016] Referring now to Figure 2, an exemplary embodiment of storage queue A 16 ("queue 16") is shown in greater detail. As can be seen, alternating packets of red 34, green 32 and blue 30 video data are individually received by queue A 16 in a sequential fashion. In this embodiment, each received packet generally comprises one 128-bit word, where each 128-bit word comprises 16 pixels of the same color, and queue 16 comprises a 240 x 128 bit memory 36 to store up to 240 packets of data. Obviously, other packet and memory sizes could be utilized. On the input, or write side of queue 16, a linear addressing system 45 stores the packets in memory 36 with a linear increment of one (i.e., the packets are stored contiguously in the order in which they are received).

[0017] On the output, or read side of queue 16, a modulo-3 addressing system 38 is utilized to select color specific sets of data that are to be burst to shared memory

18. The ability to burst color specific sets of data (e.g., red data set 42) is particularly advantageous in a color sequential system in which the three primary colors (red, green and blue) must be separated and stored at contiguous locations in the shared memory 18 in anticipation of different display presentation times.

[0018] Thus, as source video 12 arrives, it is parsed into alternating 128-bit words 36 of red, green and blue and stored in memory 36 of queue 16 using linear addressing (0, 1, 2, ...). The addressing sequence used to read data out of queue 16 is modulo-3 with a different starting value for each color (e.g., red=0, green=1, blue=2). Therefore, the first burst for a set of red data packets 42 from queue 16 to shared memory 18 will be addressed as 0, 3, 6, 9 The second burst (not shown) for a set of green data packets will have an address sequence of 1, 4, 7, 10, ... ; and the third burst (not shown) for a set of blue data packets will have an address sequence of 2, 5, 8, 11,

[0019] In a video display application having a line size of 1280 pixels, the shared memory bus is preferably 128-bits wide to meet the bandwidth requirements. Accordingly, for this exemplary embodiment, queue 16 utilizes a 240 x 128-bit architecture. Thus, three "virtual" FIFO's (red, green, and blue), each with a size of 80 x 128-bits are created using a single dual port memory. Obviously, the invention is not limited to a particular architecture as other memory sizes can be utilized to meet the particular requirements of a specific application.

[0020] In accordance with the invention, any practical burst size (e.g., 10 - 80 words) could be utilized. However, in this embodiment, a burst size of 40 words is utilized, therefore requiring 6 bursts to empty queue 16. In order to decrease the possibility of overflow of any of the colors, which could occur by leaving data in the queue too long, a scheduler 44 may be utilized to alternate colors on a round-robin basis, i.e., red 40, green 40, blue 40, red 40, green 40, blue 40.

[0021] Scheduler 44 also is responsible for granting access to shared memory 18. Specifically, scheduler 44 monitors a fullness 26, 28 of each queue 16, 22 (Figure 1) and grants access to shared memory 18 for one of the queues when the queue fullness 26, 28 exceeds a predetermined threshold. Fullness may be determined by fullness monitor 40, which may for example count write and read transactions and calculate the number of unread words. Note however that because of the asymmetric addressing (i.e., modulo-3) used in the invention, the fullness threshold must be

carefully selected. Namely, the fullness threshold must be selected on a case-by-case basis and will depend on the ratio of display bandwidth to source bandwidth, as well as the size of the queue.

[0022] The following is one exemplary embodiment for calculating a fullness threshold FT for storage queue 16 described above.

[0023] $FT = 240 * (1 - (Sf * Fcs / Bf * Fcm))$,

Where:

[0024] Fcs is the source clock frequency;

[0025] Fcm is the memory clock frequency;

[0026] Sf is a source efficiency factor (e.g., .75 indicating that a word is loaded three of every four clocks); and

[0027] Bf is the burst factor: $BL / (BL + 8)$ where BL is the burst length and 8 is the approximate overhead between bursts.

[0028] Thus, for example, the fullness threshold FT for a queue having a source clock of 27 MHz, a memory clock of 68 MHz, and a burst length of 40 would be calculated as follows:

[0029] $FT = 240 * (1 - (0.75 * 27) / (0.833 * 68)) = 154$,

where $Bf = 40 / 48 = 0.833$.

[0030] Note that this calculation provides a minimum threshold at which reading of queue 16 should start (i.e., start reading from queue 16 when more than 154 words are stored in the queue). If reading starts sooner, then some of the data from the previous row may be read again (underflow). On the other hand, in order to guard against overflow, a maximum threshold should also be considered, i.e., the point at which reading the data is so late that some data from the new row will be skipped.

[0031] Referring now to Figure 3, an alternate embodiment of a storage queue memory system 48 is shown. In this case, the alternating color packets are input 49 to a mapping system 50 that maps the sequence color packets to color specific portions of the memory 52. Thus, all red color data is stored in the first 80 address locations (0-79), all green color data is stored in the next 80 address locations (80-159) and all blue color data is stored in the final 80 address locations (160-239). A linear read system 54 is then utilized, with an increment of 1, to address color-specific sets of color packets 52 from each color specific area of the memory 52.

[0032] Referring to Figure 4, a flow diagram of the queue read control method is depicted. Control of these actions may be implemented by a state machine (not shown) in the scheduler 44. First, the fullness of the queue 16 is continuously checked 60. When the threshold is exceeded, a request for bus access for red is made 62. When the request is granted, a burst of red is transferred to the shared memory 64. After the transfer is done, a check is made to see if the full row has been transferred 74. If the full row has not been transferred, then a bus request for green is made 66. When the request is granted, green is transferred 68. Again, after the transfer is done, a check is made to see if the full row has been transferred 74. If the full row has not been transferred, then a bus request for blue is made 70. When the request is granted, a burst of blue is transferred to the shared memory 72. Again, after the transfer is done, a check is made to see if the full row has been transferred 74. If the full row has not been transferred, then a bus request for red is made 70, etc. If during any check it is determined that a full row has been transferred, then the state machine returns to a check fullness state 60.

[0033] The foregoing description of the preferred embodiments of the invention has been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teachings. Such modifications and variations that are apparent to a person skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims.

CLAIMS

1. A storage queue [16] for a color sequential display system, wherein the storage queue [16] is coupled to a shared memory [18] and comprises:
 - a system [45, 50] for receiving and storing individual packets of alternating red, green and blue video data [30, 32, 34] in the storage queue [16]; and
 - a system [38, 54] for reading out separate sets of red packets, green packets and blue packets from the storage queue [16] to the shared memory [18].
2. The storage queue [16] of claim 1, wherein the each packet comprises a word of color-specific video data.
3. The storage queue [16] of claim 2, wherein each word comprises 128 bits.
4. The storage queue [16] of claim 1, wherein:
 - each received packet is stored in a linear addressing fashion; and
 - sets of packets are read out using a modulo-3 addressing sequence.
5. The storage queue [16] of claim 1, wherein:
 - each received packet is mapped to a color specific portion of the storage queue [16]; and
 - sets of packets are read out of the color specific portion using a linear addressing sequence.
6. The storage queue [16] of claim 1, wherein the storage queue [16] comprises a single dual port memory.
7. The storage queue [16] of claim 1, wherein each set of packets comprises between 10 and 80 packets.
8. The storage queue [16] of claim 1, further comprising a fullness detection system [40] that determines when sets of packets are to be read from the storage queue [16] based on a predetermined threshold.

9. A method of managing color sequential display data in a storage queue [16] that is coupled to a shared memory [18], comprising:

receiving and storing individual packets of alternating red, green and blue video data [30, 32, 34] in the storage queue [16]; and

reading out separate sets of red packets, green packets and blue packets from the storage queue [16] to the shared memory [18].

10. The method of claim 9, wherein:

each received packet is stored in a linear addressing fashion; and

sets of packets are read out using a modulo-3 addressing sequence.

11. The method of claim 9, wherein:

each received packet is mapped to a color specific portion of the storage queue [16]; and

sets of packets are read out of the color specific portion using a linear addressing sequence.

12. The method of claim 9, wherein each set of packets is burst to the shared memory [18].

13. The method of claim 9, wherein each packet includes a 128-bit word of color-specific data, and each set of packets includes between 10 and 80 words.

14. The method of claim 9, further including the steps of:

measuring a fullness of the storage queue [16] as data is being received by the storage queue [16]; and

causing data to be read out after fullness exceeds a threshold.

15. A memory management system for use in color sequential display, comprising:
a shared memory [18]; and
a storage queue [16] coupled to the shared memory [18], wherein the storage queue [16] includes:
a system [45, 50] for receiving and storing individual packets of alternating color-specific video data in the storage queue [16]; and
a system [38, 54] for bursting separate sets of color-specific packets from the storage queue [16] to the shared memory [18].
16. The memory management system of claim 15, wherein the shared memory [18] comprises a frame memory implemented as a double data rate synchronous dynamic random access memory (DDR-SDRAM).
17. The memory management system of claim 15, wherein the storage queue [16] is implemented as a dual port memory.
18. The memory management system of claim 17, wherein the dual port memory stores each packet with a linear increment of 1 addressing mode and reads sets of packets out using a modulo-3 addressing sequence.
19. The memory management system of claim 17, wherein the dual port memory maps each received packet to a color specific portion of the storage queue [16], and reads out sets of packets using a linear addressing sequence.
20. The memory management system of claim 17, wherein the dual port memory comprises a 240 x 128 bit static random access memory.
21. The memory management system of claim 17, further comprising:
a fullness monitor [40] that measures a fullness of the storage queue [16]; and
a scheduler [44] that grants access to the shared memory [18] when the fullness exceeds a predetermined threshold.
22. The memory management system of claim 21, wherein the predetermined threshold FT is calculated using the formula:

$$FT = 240 * (1 - (Sf * Fcs / Bf * Fcm)),$$

where, Fcs is a source clock frequency; Fcm is a memory clock frequency; Sf is a source efficiency factor, and Bf is the burst factor defined as $BL/(BL + n)$ where BL is the burst length and n is the approximate overhead between bursts.

23. The memory management system of claim 22, wherein n equals 8.

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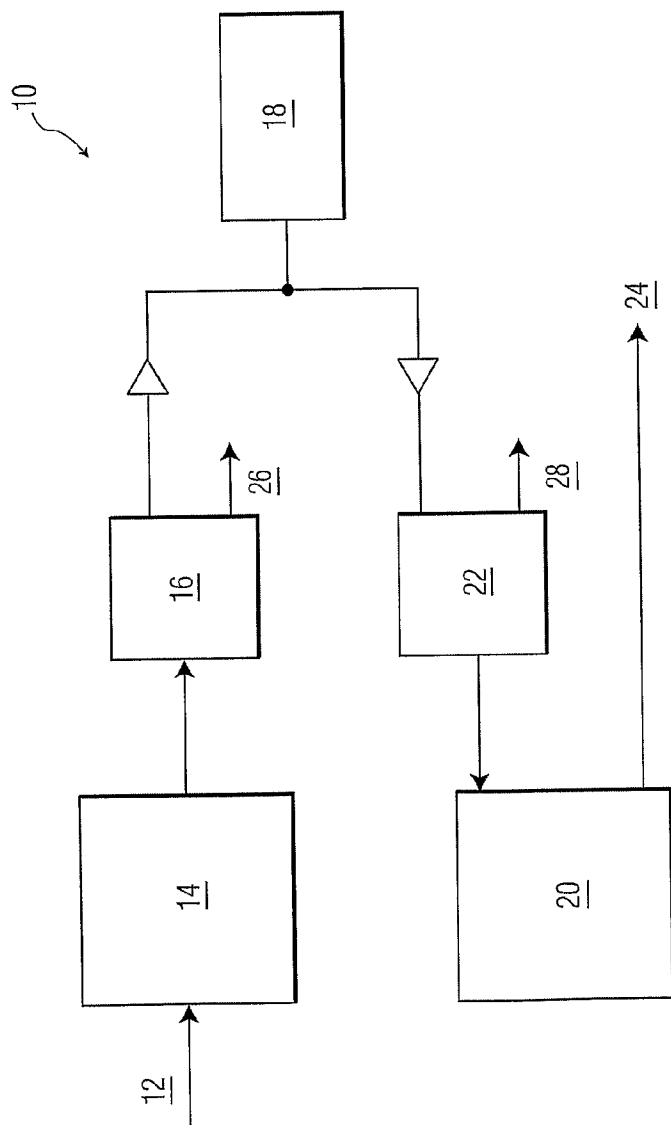
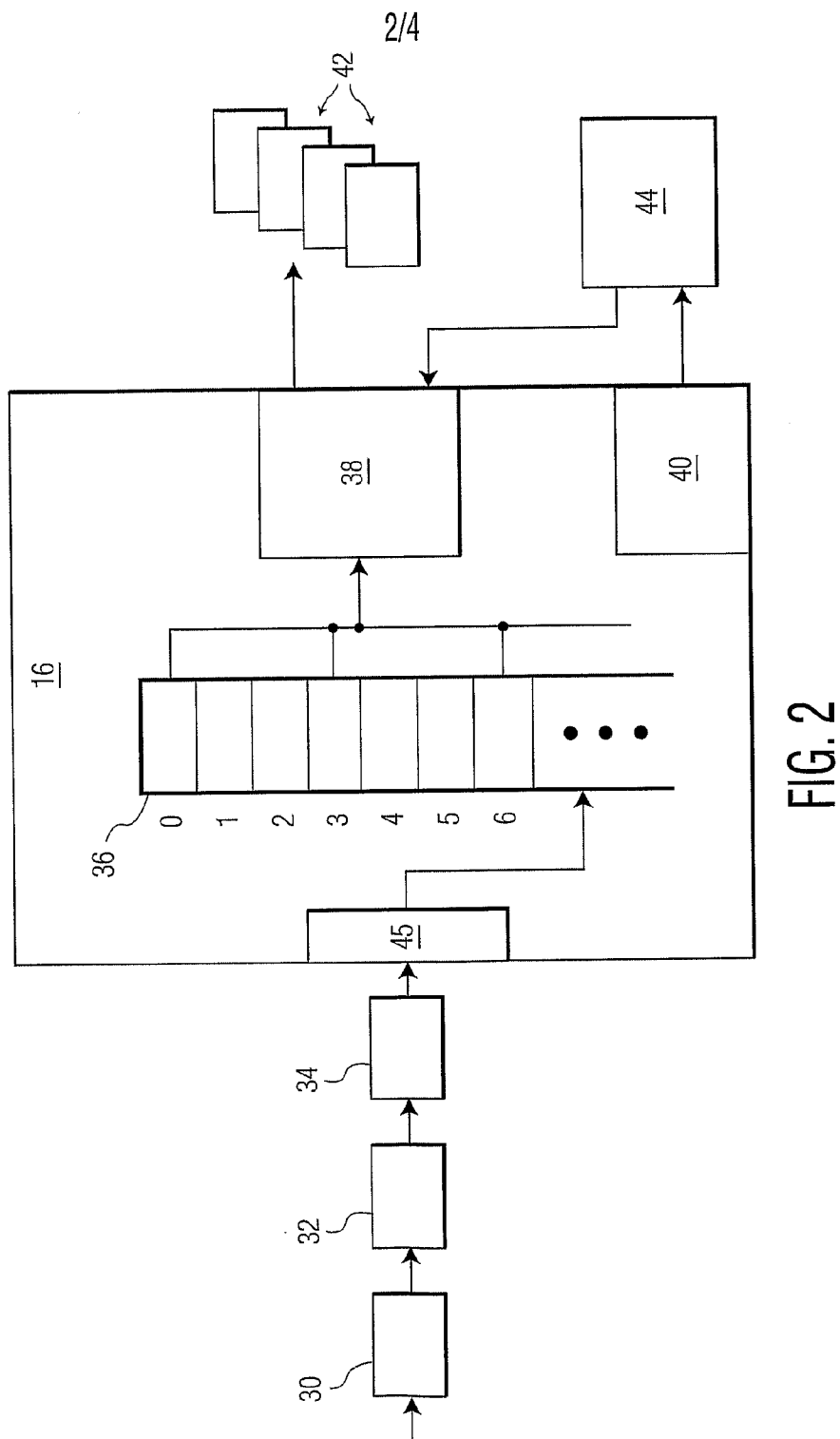


FIG. 1



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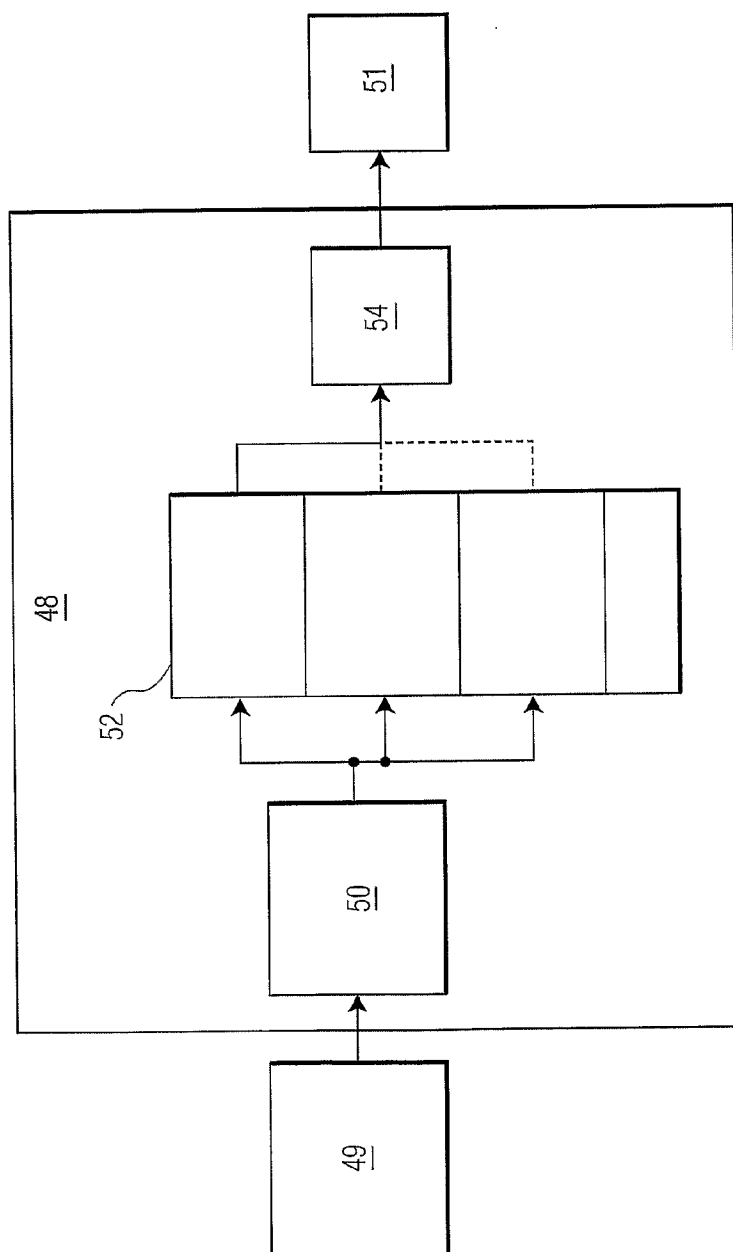


FIG. 3

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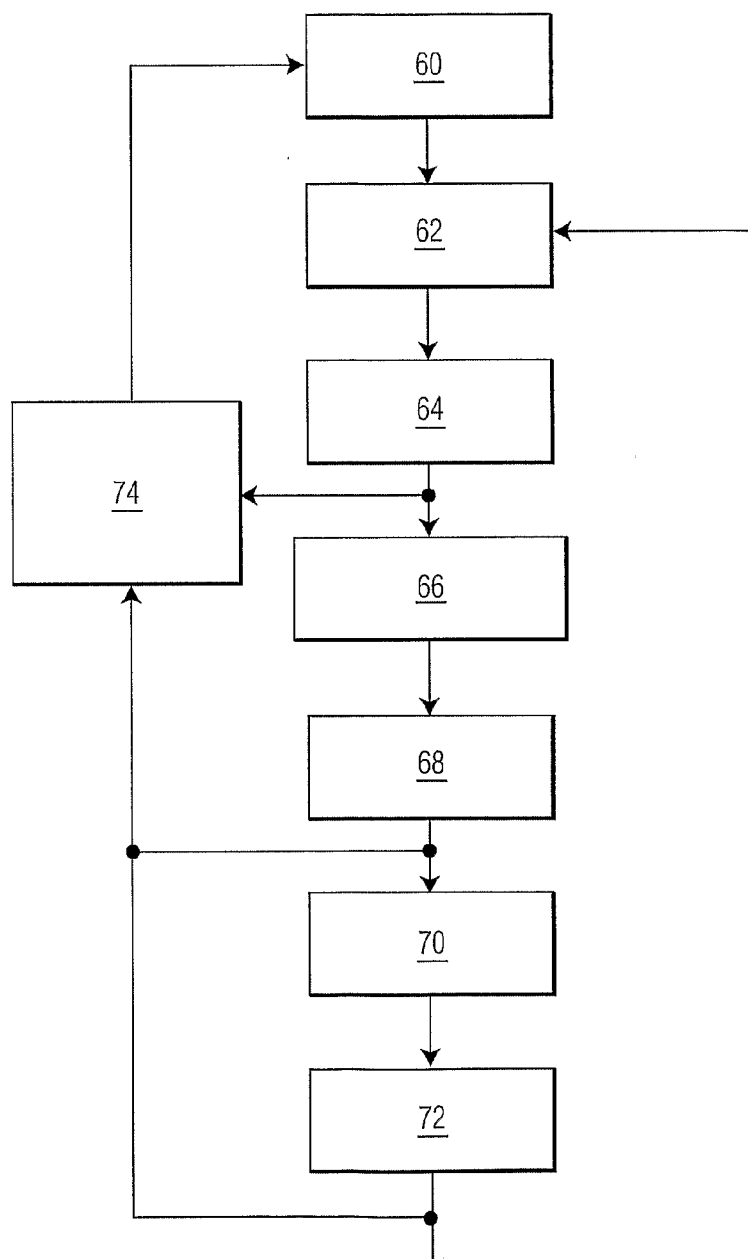


FIG. 4

INTERNATIONAL SEARCH REPORT

Int l Application No

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A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 G09G5/393 G09G5/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G09G G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 909 225 A (MARTIN ROBERT J ET AL) 1 June 1999 (1999-06-01)	1-3, 5-9, 11-17, 19-23
Y	column 4, line 57 -column 5, line 22 column 5, line 51 -column 7, line 26; figures 1-6 --- -/-	4, 10, 18



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/IB 03/03396

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	<p>GLEERUP T ET AL: "MEMORY ARCHITECTURE OF EFFICIENT UTILIZATION OF SDRAM: A CASE STUDY OF THE COMPUTATION/MEMORY ACCESS TRADE-OFF"</p> <p>PROCEEDINGS OF THE 8TH. INTERNATIONAL WORKSHOP ON HARDWARE/SOFTWARE CODESIGN: CODES 2000. SAN DIEGO, CA, MAY 3 - 5, 2000, PROCEEDINGS OF THE INTERNATIONAL WORKSHOP ON HARDWARE/SOFTWARE CODESIGN, NEW YORK, NY: ACM, US, 3 May 2000 (2000-05-03), pages 51-55, XP000966198</p> <p>ISBN: 1-58113-214-X</p> <p>page 53, right-hand column, paragraph 4</p> <p>page 54, left-hand column, paragraph 2</p> <p>-page 54, right-hand column, paragraph 1; figures 5,6</p> <p>---</p>	1-3,9, 11-13, 15-17
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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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